Alpha Bridge
AB-QSFP 28-10
Datasheet

Description

The 100Gb/s QSFP28 LR4 transceiver is compliant with the QSFP28 MSA and IEEE 802.3ba. QSFP28 LR4 transceiver modules are designed for use in 100 Gigabit Ethernet interfaces over single mode fiber.

Features

- Hot-pluggable QSFP28 form factor
- Supports 103.1Gb/s aggregate bit rates
- Maximum link length of 10km on Single Mode Fiber (SMF)
- Power dissipation < 3.5W
- Built-in digital diagnostic functions
- Built-in CDR
- 4x25.78Gb/s DFB-based LAN-WDM transmitter
- Duplex LC receptacles
- Single 3.3V power supply
- RoHS compliant
- Operating case temperature: 0~+70°C

Application

- 100GBASE-LR4 100G Ethernet

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	Ts	-40	-	85	°C	
Maximum Supply Voltage	Vcc	-0.3	-	3.6	V	
Operating Relative Humidity	RH	15	-	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Data Rate	DR	25.78±100ppm			Gb/s	1
Bit Error Rate-25.78Gb/s	BER			1E-12		2
Operating Case Temperature	Tcase	0		70	°C	
Fiber Length on SMF	L			10	km	

Notes:

1. Supports 100GBASE-LR4 per IEEE 802.3ba.
2. Tested with a $2^{31} - 1$ PRBS.

Pin Descriptions

Pin	Symbol	Name/Description	Ref.
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	

7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3 V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	2
29	Vcc Tx	+3.3 V Power supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Note:

1. Circuit ground is internally isolated from chassis ground.

2. IntL is an open collector/drain output, which should be pulled up with a 4.7k – 10k Ohms resistor on the host board. The INTL pin is de-asserted "High" after completion of reset when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

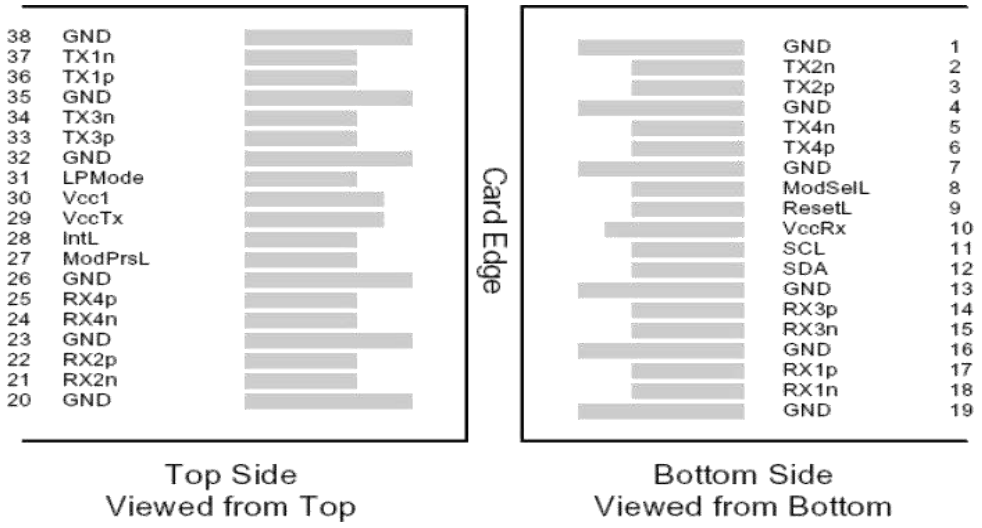


Figure 1 – QSFP28-Compliant 38-Pin Connector (Per SFF-8679)

Electrical Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Supply Voltage	Vcc	3.135		3.465	V	
Supply Current	Icc			1.12	A	
Module Total Power	P			3.5	W	1
Transmitter						
Signaling rate per lane		25.78±100ppm			Gb/s	
Differential input impedance	Zin	100	100		Ohm	
Differential input voltage amplitude	Vin			900	mVp-p	
Receiver						
Signaling rate per lane		25.78±100ppm			Gb/s	
Differential Output impedance	Zout		100		Ohm	
Differential output voltage amplitude	Vout	400		900	mVp-p	
Eye width		0.57			UI	
Vertical eye closure				5.5	dB	
Transition time, 20% to 80%	Tr/Tf	12			ps	

Notes: Maximum total power value is specified across the full temperature and voltage range.

Optical Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Signaling rate per lane		25.78125±100ppm			Gb/s	1
Center wavelength	λ	1294.53 – 1296.59			nm	
		1299.02 – 1301.09				
		1303.54 – 1305.63				
		1308.09 – 1310.19				
Sidemode Suppression ratio	SMSR	30			nm	
Transmit OMA per Lane	TXP	-1.3		4.5	dBm	

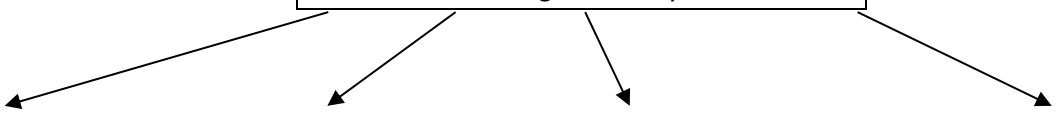
Transmit Average Power per Lane	Pout	-4.3		4.5	dBm	
Optical Extinction Ratio	ER	4			dB	
Average launch power of				-30	dBm	
Optical return loss tolerance	RL			20	dB	
Relative Intensity Noise	RIN			-130	dB/Hz	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				2
Receiver						
Signaling rate per lane		25.78125±100ppm			Gb/s	1
Center wavelength	λ	1294.53 – 1296.59			nm	
		1299.02 – 1301.09				
		1303.54 – 1305.63				
		1308.09 – 1310.19				
Average Receive Power per Lane	RXP	-10.6		4.5	dBm	
Receive Power (OMA) per Lane	RxOMA			4.5	dBm	
Receiver Reflectance	Rfl			-26	dB	
Receive Sensitivity in OMA, each Lane	SEN			-8.6	dBm	
LOS De-Assert	LOSD			-11.6	dBm	
LOS Assert	LOSA	-24			dBm	
LOS Hysteresis	LOSh	0.5			dB	

Notes:

1. Transmitter and Receiver consists of 4 lasers and photodiode operating at 25.78Gb/s each for 100GBASE-LR4,
2. Hit ratio 5E-5.

Digital Diagnostic Functions

2-Wire Serial Address 1010000x
Lower Page 00h
0 Identifier
1-2 Status
3-21 Interrupt Flags
22-33 Free Side Device Monitors
34 -81 Channel Monitors
82- 85 Reserved
86- 98 Control
99 Reserved
100-104 Hardware Interrupt Pin Masks
105-106 Vendor Specific
107 Reserved
108-110 Free Side Device Properties
111-112 Assigned for use by PCI Express
113 Free Side Device Properties
114-118 Reserved
119-122 Password Change Entry Area (Optional)
123-126 Password Entry Area (Optional)
127 Page Select Byte

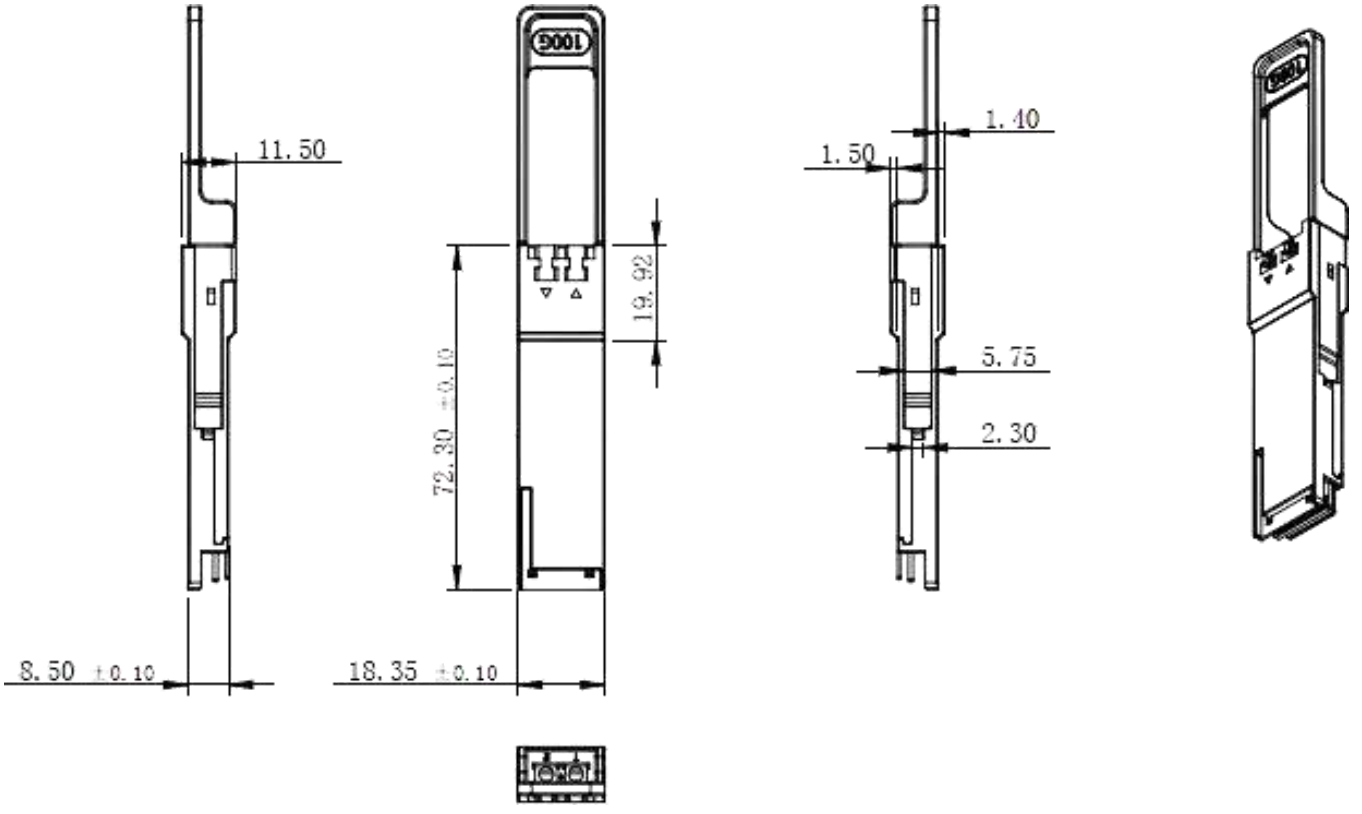


	Optional	Optional	Optional
Upper Page 00h	Page 01h	Page 02h	Page 03h
128 Identifier	128 CC_APPS	128-255 User EEPROM Data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		
	130-131 Application code entry 0		
	132-133 Application code entries 1		
192-223 Extended ID			176-223 Channel Thresholds
224-255 Vendor-Specific ID			224 Tx EQ & Rx
	134-253 other entries		Emphasis Magnitude ID
			225 RX output amplitude indicators
			226-241 Channel Controls
			242-251 Channel Monitor Masks
	254-255 Application Code Entry TL		252-255 Reserved

Figure 2 – Two-Wire Interface Fields

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. The 2-wire serial interface shall consist of a master and slave. The fixed side shall be the master and the free side shall be the slave. Control and data are transferred serially. The master shall initiate all data transfers. Data can be transferred from the master to the slave and from the slave to the master. The 2-wire interface shall consist of clock (SCL) and data (SDA) signals. The master utilizes SCL to clock data and control information on the 2-wire bus. The master and slave shall latch the state of SDA on the positive transitioning edge of SCL. The SDA signal is bi-directional. During data transfer, the SDA signal shall transition when SCL is low. A transition on the SDA signal, while SCL is high, shall indicate a stop or start condition.

Mechanical Specifications



Ordering information

Part Number	Description
AB-QSFP28-10	100Gbps QSFP28 LAN WDM4, LC, 10km, 0°C~+70°C, with DDM

Note: All information contained in this document is subject to change without notice